UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,789	03/16/2004	Andy Yu	M-16550 US	3122

32605 7590 11/22/2006

MACPHERSON KWOK CHEN & HEID LLP
2033 GATEWAY PLACE
SUITE 400
SAN JOSE, CA 95110

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,789	YU ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,15-17 and 41-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,15-17 and 41-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 14, 2006 has been entered.

Status of the Claims

2. Amendment filed August 14, 2006 has been entered. Claims 12-14 and 18-40 have been cancelled. Claims 1-4, 6, 8-11, 15, 16, 41-44, 46, 48-53, 55-58 and 60-67 have been amended. Claims and 1-11, 15-17 and 41-68 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung (U.S. Patent No. 6,018,178) in view of Pan (U.S. Patent No. 5,760,435) all of record.

With respect to claim 1, Sung teaches an electrically alterable memory device substantially as claimed including:

a first semiconductor layer (2) doped with a first dopant (N) in a first concentration;

a second semiconductor layer (3), doped with a second dopant (P), the second semiconductor layer (3) having a top side;

two spaced-apart diffusion regions (14) embedded in the top side of the second semiconductor layer (3), each diffusion region (14) doped with the first dopant (N) in a second concentration greater than the first concentration, the two diffusion regions (14) including a first diffusion region (14aa) and a second diffusion region (14ab), and with a first channel region defined therebetween;

a first floating gate (10A) having a first height and comprising a conductive material, the first floating gate (10A) being disposed adjacent the first diffusion region (14aa) and above the first channel region, separated therefrom by a first insulator region (9), the first floating gate (10A) capable of storing electrical charge;

a second floating gate (10B) having a second height and comprising of a conductive material, the second floating gate (10B) being disposed adjacent the second diffusion region (14ab) and above the first channel region and separated therefrom by a second insulator region (9), the second floating gate (10B) capable of storing electrical charge; and

a control gate (5) having a third height and comprising of a conductive material, the control gate (5) being disposed laterally between the first floating gate (10A) and the second floating gate (10B), the control gate (5) being separated from the first floating gate (10A) by a first vertical insulator layer (8) and being separated from the second floating gate (10B) by a second vertical insulator layer (8), the control gate (5) acting as a word select line, the control gate (5) further being disposed above the first channel region without overlapping the two

spaced-apart diffusion regions (14), being separated therefrom by a third insulator region (4). (See Figs. 1 and 9).

Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the third height is higher than the first and second heights.

However, Pan teaches an electrically alterable memory device having a control gate (30), first (61) and second (62) floating gates formed on a semiconductor substrate (10), wherein the control gate (30) has a third height that is higher than both first (61) and second (62) floating gates. (See Fig. 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung higher than the first and second floating gates as taught by Pan to double storage efficiency.

With respect to claim 2, the first dopant and the second dopant of Sung or Pan are N-type and P-type, respectively.

Thus, Sung and Pan are shown to teach all the features of the claim with the exception of alternatively utilizing opposite dopants type.

However, it is well known in the art that dopant N-type or P-type can be used interchangeably to form different characteristics devices, e.g., N channel or P channel devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to utilize P-type and N-type, respectively for the first and second dopants of Sung or Pan since it has been held that a mere reversal of the essential working parts, e.g., N-type instead

of P-type or vice versa, of a device involves only routine skill in the art. *In re Einstein*, 8 USPQ 167.

With respect to claim 3, the first dopant of Sung has an N-type characteristic and the second dopant having a P-type characteristic.

With respect to claims 4 and 6, the first and second insulator region (9) of Sung have the thickness that allows tunneling of charge between the first (10A) and second (10B) floating gates and the first channel region.

With respect to claims 5 and 7, in view of Pan, the thickness of the first and second insulator region (50) are between 80 Å to 120 Å, thus, overlaps the claimed range between 70 Å and 110 Å.

With respect to claims 8-11, the first and second vertical insulator (8) of Sung is made from a silicon dioxide or in view of Pan, oxide-nitride-oxide (ONO) having a thickness that provides capacitance between the first floating gate (10A) and second floating gate (10B) and the control gate (5), respectively, and the first and second vertical insulator (8) prevents leakage between the first (10A) and second (10B) floating gates and the control gate (5), respectively.

With respect to claims 15, the first and second floating gate (10) of Sung or Pan are each inherently capable of storing multiple levels of charge.

With respect to claim 16, the first and second floating gate (10) of Sung or Pan are each inherently capable of storing four levels of charge.

With respect to claim 17, an oxide layer (9) of Sung is disposed on top of each diffusion region (14).

4. Claims 41-48, 50 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 in view of Chen et al. (U.S. Patent No. 6,271,089) of record.

With respect to claim 41, Sung teaches an electrically alterable memory device substantially as claimed including:

a first semiconductor layer (2) doped with a first dopant in a first concentration;

a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant that has an opposite electrical characteristics that the first dopant, the second semiconductor layer (3) having a top side;

two spaced-apart diffusion regions (14) embedded in the top side of the second semiconductor layer (3), each diffusion region being doped with the first dopant in a second concentration greater than the first concentration, the two diffusion regions (14) including a first diffusion region (14aa) and a second diffusion region (14ab), with a first channel region defined therebetween;

a first floating gate (10A) having a left side and a right side and comprising a conductive material, the first floating gate (10A) being disposed adjacent the first diffusion region (14aa) and above the first channel region and being separated therefrom by a first insulator region (9), the first floating gate (10A) being capable of storing electrical charge;

a second floating gate (10B) having a left side and a right side and comprising of a conductive material, the second floating gate (10B) being disposed adjacent the second diffusion region (14ab) and above the first channel region and being separated therefrom by a second

insulator region (9), the second floating gate (10B) being capable of storing electrical charge; and

a control gate (5) comprising of a conductive material, the control gate (5) being disposed laterally between the first (10A) and second (10B) floating gate, the control gate (5) being separated from the first floating gate (10A) by a third insulator layer (8) and being separated from the second floating gate (10B) by a fourth insulator layer (9), the control gate (5) further being disposed above the first channel region and separated therefrom by a third insulator region (4). (See Figs. 2 and 9).

Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the control gate covering the first and second floating gate on at least right side and left side.

However, Chen teaches the control gate (208) of electrically alterable memory device covering the first (204a) and second (204b) floating gate on at least right side and left side. (See Fig. 2B).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung to cover the first and second floating gates on at least right side and left side as taught by Chen to increase the numbers of bits stored in the unit area of a flash memory.

With respect to claim 42, the first dopant and the second dopant of Sung or Chen are N-type and P-type, respectively.

Thus, Sung and Chen are shown to teach all the features of the claim with the exception of alternatively utilizing opposite dopants type.

However, it is well known in the art that dopant N-type or P-type can be used interchangeably to form different characteristics devices, e.g., N channel or P channel devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to utilize P-type and N-type, respectively for the first and second dopants of Sung or Chen since it has been held that a mere reversal of the essential working parts, e.g., N-type instead of P-type or vice versa, of a device involves only routine skill in the art. *In re Einstein*, 8 USPQ 167.

With respect to claim 43, the first dopant of Sung has an N-type characteristic and the second dopant having a P-type characteristic.

With respect to claims 44 and 46, the first and second insulator region (9) of Sung having a thickness that allows tunneling of charge between the first and second floating gate (10) and the first channel region.

With respect to claims 45 and 47, the thickness of the first and second insulator region (9) of Sung are between 60 Å to 70 Å, thus includes lower end of the claimed range between 70 Å and 110 Å.

With respect to claims 48 and 50, the third and fourth insulator (8) of Sung or Chen are made from a silicon dioxide having a thickness that provides capacitance between the first and second floating gate (10) and the control gate (5), respectively, and wherein the third and fourth

insulator (8) prevents leakage between the first and second floating gate (10) and the control gate (5), respectively.

With respect to claim 52, the first and second floating gate (10) of Sung or Chen are each inherently capable of storing multiple levels of charge.

With respect to claim 53, the first and second floating gate (10) of Sung or Chen are each inherently capable of storing four levels of charge.

With respect to claim 54, an oxide layer (9) of Sung or Chen is disposed on top of each diffusion region (14).

5. Claims 49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 and Chen '089 as applied to claim 41 above, and further in view of Pan '435.

The third and fourth insulator (8) of Sung or Chen are made from a silicon dioxide having a thickness that provides capacitance between the first and second floating gate (60) and the control gate (66), respectively, and the first and second vertical insulator (64) preventing leakage between the first and second floating gate (60) and the control gate (66), respectively.

Thus, Sung and Chen are shown to teach all the features of the claim with the exception of utilize Oxide-Nitride-Oxide (ONO) for the third and fourth insulator.

However, Pan teaches ONO or silicon oxide can be used for the third and fourth insulator (40'). (See Fig. 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to use ONO for the third and fourth insulator of Sung or Chen as taught

by Pan to prevents leakage between the first and second floating gates (10) and the control gate (5) since the materials are well known in the art to be used interchangeably.

Further, it has been held to be within the general skill of a worker in the art to select a known material, e.g., O-N-O, on the basis of it suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416., 125 USPQ 416.

6. Claims 55-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sung '178 in view of Hong (U.S. Patent No. 5,576,232) of record.

With respect to claim 55, Sung teaches an electrically alterable memory device substantially as claimed including:

a first semiconductor layer (2) doped with a first dopant in a first concentration;

a second semiconductor layer (3), adjacent the first semiconductor layer (2), doped with a second dopant that has an opposite electrical characteristics than the first dopant, the second semiconductor layer (3) having a top side;

two spaced-apart diffusion regions (14) embedded in the top side of the semiconductor layer (3), each diffusion region (14) being doped with the first dopant in a second concentration, the two diffusion regions including a first diffusion region (14aa) and a second diffusion region (14ab), with a first channel region defined between the first (14aa) and second (14ab) diffusion region;

a first floating gate (10A) comprising a conductive material, the first floating gate (10A) being disposed adjacent the first diffusion region (14aa) and above the first channel region and

being separated therefrom by a first insulator region (9), the first floating gate (10A) being capable of storing electrical charge;

a second floating gate (10B) comprising a conductive material, the second floating gate (10B) being disposed adjacent the second diffusion region (14ab) and above the first channel region and being separated therefrom by a second insulator region (9), the second floating gate (10B) being capable of storing electrical charge; and

a control gate (5) having at least two lateral sides and comprising of a conductive material, the control gate (5) being disposed laterally between the first (10A) and second (10B) floating gate, the control gate (5) being separated from the first floating gate (10A) by a first vertical insulator layer (8) and being separated from the second floating gate (10B) by a second vertical insulator layer (8), the control gate being separated from the first channel region by a third insulator region (4). (See Fig. 7h).

Thus, Sung is shown to teach all the features of the claim with the exception of explicitly disclosing the control gate being covered by the first and second floating gates on more than one lateral side.

However, Hong teaches the control gate (520) of the electrically alterable memory device being covered by the first floating gate (580) and second floating gate (580) on more than one lateral side. (See Fig. 7H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the control gate of the electrically alterable memory device of Sung being

covered on more than one lateral side by the first and second floating gates as taught by Hong to improve device reliability.

With respect to claim 56, the first dopant and the second dopant of Sung or Hong are N-type and P-type, respectively.

Thus, Sung and Hong are shown to teach all the features of the claim with the exception of alternatively utilizing opposite dopants type.

However, it is well known in the art that dopant N-type or P-type can be used interchangeably to form different characteristics devices, e.g., N channel or P channel devices.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to utilize P-type and N-type, respectively for the first and second dopants of Sung or Hong since it has been held that a mere reversal of the essential working parts, e.g., N-type instead of P-type or vice versa, of a device involves only routine skill in the art. *In re Einstein*, 8 USPQ 167.

With respect to claim 57, the first dopant of Sung or Hong has an N-type characteristic and the second dopant having a P-type characteristic.

With respect to claims 58 and 60, the first and second insulator region (9) of Sung or Hong have thicknesses that allows tunneling of charge between the first (10A) and second (10B) floating gate and the first channel region.

With respect to claims 59 and 61, in view of Hong, the first and second insulator region (57) have the thickness of 60 Å to 100 Å, hence overlaps the claimed range between 70 Å and 110 Å.

With respect to claims 62-65, the first and second vertical insulator (8) of Sung is made from a silicon dioxide or in view of Hong, oxide-nitride-oxide (ONO) having a thickness that provides capacitance between the first floating gate (10A) and second floating gate (10B) and the control gate (5), respectively, and the first and second vertical insulator (8) prevents leakage between the first (10A) and second (10B) floating gates and the control gate (5), respectively.

With respect to claim 66, the first (10A) and second (10B) floating gates of Sung or Hong are each inherently capable of storing multiple levels of charge.

With respect to claim 67, the first (10A) and second floating gate (580) of Sung or Hong are each inherently capable of storing four levels of charge.

With respect to claim 68, an oxide layer (9) of Sung is disposed on top of each diffusion region (14).

Response to Arguments

7. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).